#15/IDS
EV182661221US
1/14/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date . . . . . June 4, 2001
Inventor . . . . . Klaus Florian Schuegraf et al.
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2815
Examiner . . . . . E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 12-27-02

D. Brent Kenady
Reg. No. 40,045
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

01/02/2003 YPOLITE1 00000042 09875501
01 FC:1251 110.00 OP

01/02/2003 YPOLITE1 00000042 09875501
02 FC:1806 180.00 OP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/332,271
Priority Filing Date ..... June 11, 1999
Inventor ..... Klaus Florian Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2815
Priority Examiner ..... E. Lee
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional of co-pending Application Serial No. 09/332,271, filed on June 11, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 6-4-01

Attorney: _____
D. Brent Kenady
Reg. No. 40,045

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
MI22-1741	09/875,504
APPLICANT: Klaus Florian Schuegraf et al.	
FILING DATE: June 4, 2001	GROUP: 2815

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,767,558	06/16/98	Lo et al.			
	AB	5,208,182	05/04/93	Narayan et al.			
	AC	5,877,074	03/02/99	Jeng et al.			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AM		Wolf et al., "Silicon Processing for the VLSI Era - Volume 1: Process Technology," ©1986 Lattice Press, pages 384-385 (4 pages total)
	AN		
	AO		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EL46 780540

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
MI22-1741	Filed Herewith
APPLICANT	
Klaus Florian Schuegraf et al.	
FILING DATE	GROUP
Filed Herewith	Unknown

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,425,392	06/95	Thakur et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AK		Taishi Kubota et al.; "The Effect of the Floating Gate/Tunnel SiO_2 Interface on FLASH Memory Data Retention Reliability"; 1994; 2 pages
	AL		Shoue Jen Wang et al.; "Effects of Poly Depletion on the Estimate of Thin Dielectric Lifetime"; IEEE Electron Device Letters, Vol. 12, No. 11, November 1991; pp. 617-619
	AM		Klaus F. Schuegraf et al.; "Impact of Polysilicon Depletion in Thin Oxide MOS Technology"; 1993; pp. 86-88
	AN		E. H. Snow et al.; "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon"; Journal of the Electrochemical Society, March 1966; pp. 263-269

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.